What is claimed is:

1. A system comprising:

an implantable medical device comprising:

a memory; and

a controller circuit, coupled to the electrical input and memory, wherein the controller circuit is operable to enter a memory scrubbing mode that increases a rate of detecting and correcting single bit errors in the memory when the controller circuit determines the implantable device is in a high-energy radiation environment.

2. The system of claim 1, wherein the controller circuit determines a high-energy radiation environment by detecting a rate of memory errors that exceeds a predetermined threshold.

3. The system of claim 1, wherein the implantable medical device further includes a sensor coupled to the controller circuit to determine the implantable device has entered a high-energy radiation environment.

4. The system of claim 3, wherein the sensor includes at least one memory cell designed to be more susceptible to radiation energy than other memory cells, and wherein the controller circuit determines a high-energy radiation environment by detecting a rate of memory errors in the memory cell that exceeds a predetermined threshold.

5. The system of claim 4, wherein the at least one memory cell designed to be more susceptible to radiation than other memory cells includes a RAM cell.

6. The system of claim 1, wherein the controller circuit is operable to exit the memory scrubbing mode when the controller circuit determines that the implantable device is no longer in a high-energy radiation environment.

7. The system of claim 6, wherein the controller circuit determines that the implantable medical device is no longer in a high-energy radiation environment by detecting a rate of memory errors that is below a predetermined threshold rate.

8. The system of claim 6, wherein the memory includes at least one memory cell designed to be more susceptible to radiation energy than other memory cells, and wherein the controller circuit determines the implantable medical device is no longer in a high-energy radiation environment by detecting a rate of memory errors in the at least one memory cell that is below a predetermined threshold rate.

9. The system of claim 8, wherein the at least one memory cell includes a plurality of memory cells designed to be more susceptible to radiation than other memory cells, and wherein such cells are distributed among a plurality of physical locations of the memory.

10. The system of claim 1, wherein the implantable medical device includes a timer coupled to the controller circuit, and wherein the controller circuit is operable to exit the memory scrubbing mode after a predetermined time duration.

11. The system of claim 1, wherein the controller circuit is operable to detect and correct single bit errors in the memory.

12. The system of claim 1, wherein the controller circuit is operable to detect and correct multiple bit errors in the memory.

13. The system of claim 1, wherein the implantable medical device further includes a telemetry circuit coupled to the controller circuit, wherein the system further includes an external device to communicate with the device through the telemetry circuit, and wherein the controller circuit determines a high-energy radiation environment by the external device enabling a high-energy radiation memory scrubbing mode in the implantable medical device.

14. The system of claim 13, wherein the controller circuit determines that the implantable medical device is no longer in a high-energy radiation environment by the external device disabling the high-energy radiation memory scrubbing mode in the implantable medical device.

15. The system of claim 13, wherein the external device is operable to communicate with a global computer network.

16. The system of claim 13, wherein the external device includes a programmer of an implantable medical device.

17. The system of claim 13, wherein the external device is an RF transmitter associated with a radiation source.

18. The system of claim 1, wherein the implantable medical device further includes:

at least one output to provide therapy to the patient; and

a therapy circuit coupled to the at least one output and the controller circuit, the therapy circuit operable to deliver therapy to the patient.

19. The system of claim 18, wherein the controller circuit is operable to execute instructions implementing the memory scrubbing mode at a lower priority than instructions related to therapy.

20. The system of claim 18, wherein the controller circuit is configured to withhold therapy when the implantable medical device enters the memory scrubbing mode.

21. The system of claim 18, wherein the implantable medical device further includes at least one electrical input to receive sensed electrical activity of a heart of a patient, wherein the output includes an electrical output, and the implantable device is a cardiac rhythm management device.

22. The system of claim 21, wherein the implantable medical device includes a cardioverter defibrillator.

23. The system of claim 19, wherein the implantable medical device provides drug therapy to the patient.

24. A method comprising:

determining that an implantable medical device is in a high-energy radiation environment;

enabling a memory scrubbing mode in response to the implantable medical device entering the high-energy radiation environment; and

increasing a rate of detecting and correcting memory errors in the device upon the enabling of the scrubbing mode.

25. The method of claim 24, wherein determining that an implantable medical device is in a high-energy radiation environment includes the implantable device detecting a rate of memory errors that exceeds a predetermined threshold.

26. The method of claim 24, wherein determining that an implantable medical device is in a high-energy radiation environment includes the implantable device detecting that at least one memory cell susceptible to lower levels of radiation energy than other memory cells has a rate of memory errors that exceeds a predetermined threshold rate.

27. The method of claim 24, wherein determining that an implantable medical device is in a high-energy radiation environment includes an external device enabling the implantable device into a high-energy radiation memory scrubbing mode.

28. The method of claim 24, wherein the method further includes disabling the memory scrubbing mode when a duration of the memory scrubbing mode in the implantable medical device exceeds a predetermined duration.

29. The method of claim 24, wherein the method further includes:

determining that the implantable medical device is no longer in the high-energy radiation environment;

disabling the memory scrubbing mode; and

returning to a lower rate of detecting and correcting memory errors in the device.

30. The method of claim 29, wherein determining that the implantable medical device is no longer in a high-energy radiation environment includes the implantable device detecting a rate of memory errors that is below a predetermined threshold.

31. The method of claim 29, wherein determining that the implantable device is no longer in a high-energy radiation environment includes detecting that at least one memory cell susceptible to lower levels of radiation energy than other memory cells has a rate of memory errors below a predetermined threshold rate.

32. The method of claim 29, wherein determining that the implantable device is no longer in a high-energy radiation environment includes an external device disabling the memory scrubbing mode.

33. A system comprising:

an implantable medical device, the implantable medical device comprising:

a memory circuit;

a radiation detector circuit to detect a condition correlative to a high-energy radiation level that exceeds a background radiation level;

a controller circuit, operatively coupled to the memory circuit and the radiation detector circuit, wherein in response to the radiation detector circuit indicating a high-energy radiation level, the controller circuit checks the memory circuit for any errors in memory and corrects any such errors.

34. The system of claim 33, wherein in response to the radiation detector circuit indicating a high-energy radiation level, the controller circuit checks the memory circuit for any errors in memory and corrects any such errors, the checking and correcting performed more frequently when the radiation detector circuit indicates a high-energy radiation level is present than when the radiation detector circuit indicates that a high-energy radiation level is not present.

35. The system of claim 33, wherein in response to the radiation detector circuit no longer indicating a high-energy radiation level, the controller circuit checks the memory circuit for any errors in memory and corrects any such errors less frequently than when the radiation detector circuit indicates that a high-energy radiation level is present.

36. The system of claim 33, wherein the radiation detector circuit includes the controller circuit and the memory circuit operating together to detect a rate of occurrence of errors in memory, wherein the controller is operable to compare a detected rate of occurrence of errors in memory in the memory circuit to a predetermined threshold value and to declare a high-energy radiation level if the detected rate exceeds the predetermined threshold value.

37. The system of claim 33, wherein in response to the radiation detector circuit indicating a high-energy radiation level, the controller circuit checks the memory circuit for any single bit errors in memory and corrects any such single bit errors.

38. A system comprising:

an implantable medical device, the implantable medical device comprising:

a memory circuit;

a controller circuit, operatively coupled to the memory circuit to detect, at a checking rate, a rate of occurrence of errors in information stored in the memory circuit, and to compare the rate of occurrence of errors to a predetermined threshold, and to increase the checking rate from a first checking rate value to a

second checking rate value in response to the rate of occurrence of the errors exceeding the predetermined threshold.

39. The system of claim 38, in which the errors in information are single bit errors and the controller is configured to correct the single bit errors.

40. The system of claim 38, wherein the information includes instructions executable by the controller circuit.

41. The system of claim 38, wherein the controller circuit is operatively coupled to the memory circuit to decrease the checking rate from a first checking rate value to a second checking rate value in response to the rate of occurrence of the errors being below the predetermined threshold.

42. The system of claim 38, wherein the system further includes a timer and the controller circuit is operatively coupled to the memory circuit to decrease the checking rate from a first checking rate value to a second checking rate value after a predetermined time.

43. A method comprising:

determining a condition correlative to a high-energy radiation level that exceeds a background radiation level;

checking a memory of an implantable medical device for any errors in stored information; and

correcting any such errors.

44. The method of claim 43, wherein determining includes detecting that a rate of occurrence of errors in stored information exceeds a predetermined rate.

45. The method of claim 43, wherein checking the memory for any errors and correcting any errors includes checking and correcting at a higher rate than a rate previous to the determining of the higher radiation level.

46. The method of claim 43, wherein determining includes detecting using a radiation detector circuit in the implantable medical device

47. A system comprising:

an implantable medical device, the implantable medical device comprising:

a memory circuit;

means for determining a condition correlative to a high-energy radiation level that exceeds a background radiation level;

a controller circuit, operatively coupled to the memory circuit and the radiation detector means, wherein in response to the radiation detector circuit indicating a high-energy radiation level, the controller circuit checks the memory circuit for any errors in memory and corrects any such errors.

48. A system comprising:

an implantable medical device comprising:

at least one electrical input, wherein the electrical input is coupled to at least one electrode, the at least one electrode to sense electrical activity of a heart;

a sensing circuit coupled to the electrical input to receive sensed electrical activity of a heart of a patient;

at least one electrical output to provide therapy to the heart;

a therapy circuit coupled to the at least one output, operable to deliver therapy to the heart;

a memory;

a radiation detector circuit;

a controller circuit, coupled to the therapy circuit, sensing circuit, radiation detector circuit and memory, wherein the controller circuit is operable to provide therapy through the therapy circuit and to enter a memory scrubbing mode that

increases a rate of detecting and correcting single bit errors in the memory when the radiation detector circuit indicates the implantable device is in a high-energy radiation environment; and

a telemetry circuit coupled to the controller; and

an external device to communicate with the implantable medical device through the telemetry circuit.

49. The system of claim 48, wherein the radiation detector circuit includes at least one memory cell designed to be susceptible to lower levels of radiation energy than other memory cells.

50. The system of claim 48, wherein the implantable device includes a cardioverter defibrillator.